eRED-DOCK

NETWORK AUDIO INTERFACE

OEM/EVALUATION BOARD DATASHEET

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eRED-DOCK-DS
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Preamble

I. About This Datasheet

This document provides the information required for integration and operation of the USB Digital Audio Interface. For more information, please refer to the product description available from the engineered SA Web site at www.engineered.ch

II. Company Information

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Routine maintenance is not required. This product is warranted to be free of any defect with respect to performance, quality, reliability and workmanship for a period of SIX (6) months from the date of shipment from engineered SA.

In case it is proven that your product is actually defective during this warranty period only, engineered SA will gladly repair or replace this piece of equipment with a unit of equal performance characteristics.

Should this product be defective after expiration of your warranty period, engineered SA will repair this piece of equipment for as long as suitable replacement components are available. You, the owner, will bear any labor and/or component costs incurred in the repair or refurbishment of the said equipment, beyond the SIX (6) months warranty period. Any attempt to repair this product by anyone during this period other than by engineered or any authorised 3rd party will void your warranty.

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VI. Documentation Release Notice

This document is under revision control and updates will only be issued as a replacement document with a new version number.

Product specifications are subject to change without notice.

1 Introduction

1.1 Highlights

The eRED-DOCK interface offers a top-notch solution for network audio playback systems, based on our Ethernet Audio Renderer Module eRED-MOD. Developed exclusively for High-End systems, it achieves jitter-free, bit-perfect playback with no compromise on sound quality. Thanks to its compatibility with the UPnP AV 2.0 standards, its integration into a home network is easy. Key features for the eRED-DOCK include:

- Digital Media Renderer for stereo audio
- UPnP AV 2.0 / DLNA
- Playing and decoding common audio formats* from HTTP streams
- 2-channel asynchronous endpoint for highest quality digital audio stereo playback
- Bit-perfect, jitter free data transmission
- Up to 32-bit resolution, sampling rate up to 384 kHz
- Support for DSD64, DSD128 and DSD256
- Support for gapless playback
- On-board 22.5792 MHz and 24.576 MHz ultra-low phase noise oscillators.
- Master clock output for DAC synchronisation
- I2S/DSD output at CMOS level
- S/PDIF and AES/EBU digital audio outputs, buffered and transformer-coupled
- Single 5V power supply

(*) Subject to licensing by the final product manufacturer for the various audio decoders.

The eRED-DOCK interface plays music from streams, from a file server or an Internet stream, acting as a UPnP AV/DLNA Media Renderer device. Common PCM (Pulse Code Modulation) audio formats are supported, including lossless FLAC up to 384kHz. One-bit DSD (Direct Stream Digital) is also supported via uncompressed DSF and DFF files.

Ethernet streaming is based on an asynchronous protocol, clocked by ultra-low jitter on-board oscillators. Using this concept, the design benefits of a local high-quality master clock to achieve highest quality, jitter-free digital audio playback.

1.2 Audio Renderer Module eRED-MOD

The eRED-MOD is the heart of the eRED-DOCK interface, a full featured and easy-to-integrate OEM solution for network audio playback systems. Our proprietary solution for network audio playback takes care of the asynchronous mode, clock management, formats decoding and UPnP/DLNA support to provide an unprecedented listening experience. Latest high-resolution files, be they DSD or PCM, can be streamed from local or remote servers with perfect clocking and data integrity. This state-of-the-art concept is the solution for network connectivity, technically the best interface for digital music reproduction, a key component for any modern High-End DAC.

1.3 Functional Block Diagram

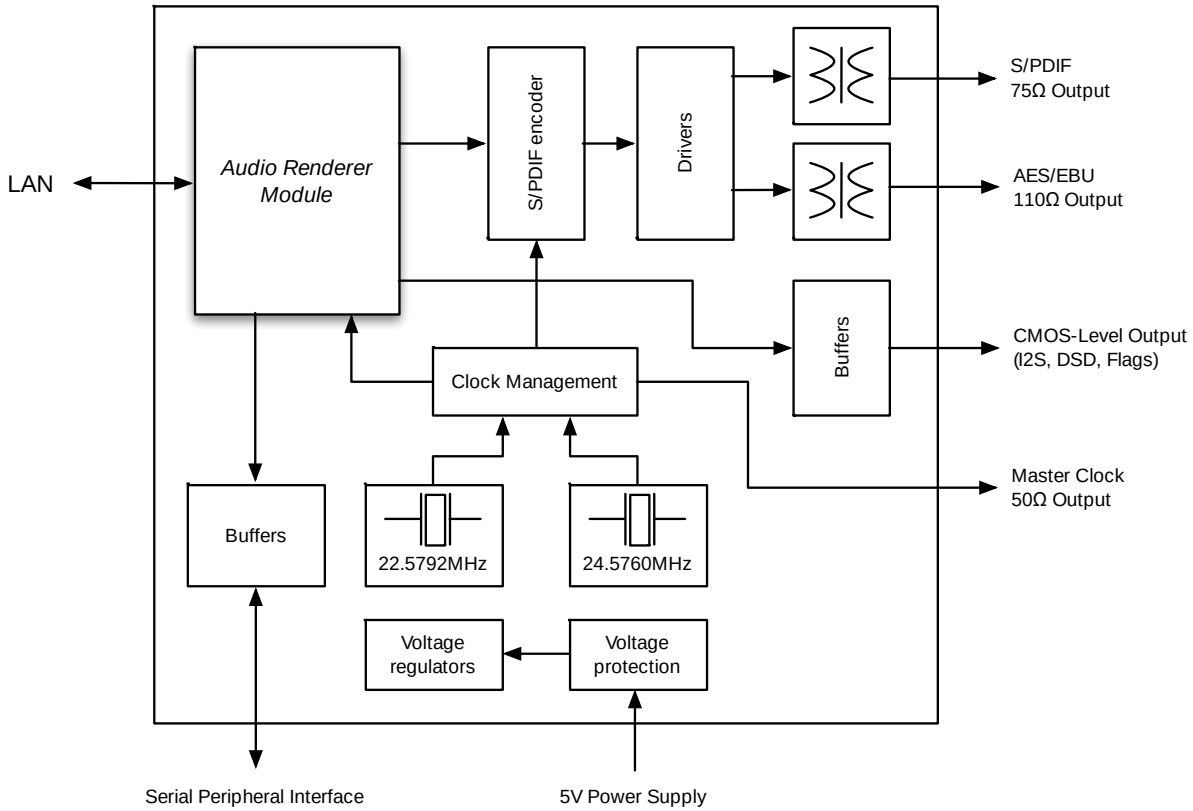

Figure 1-1 – eRED-DOCK Functional block diagram

1.4 Typical Network Audio Setup

A network audio setup is typically composed of the following devices:

- Digital Media Server (DMS) – Multimedia files are stored on this device and are made available to the network.
- Digital Media Renderer (DMR) – This device is the rendering output, able to play content from a Media Server and controlled by a Digital Control Point.
- Digital Control Point (DCP) – This device browses the content provided by Media Servers and sends commands to the Media Renderer for rendering the selected media.

Playback starts once the Control Point has sent a file path and play command to the Media Renderer. The Media Renderer fetches the file directly from the Media Server, and the data stream does not go through the Control Point.

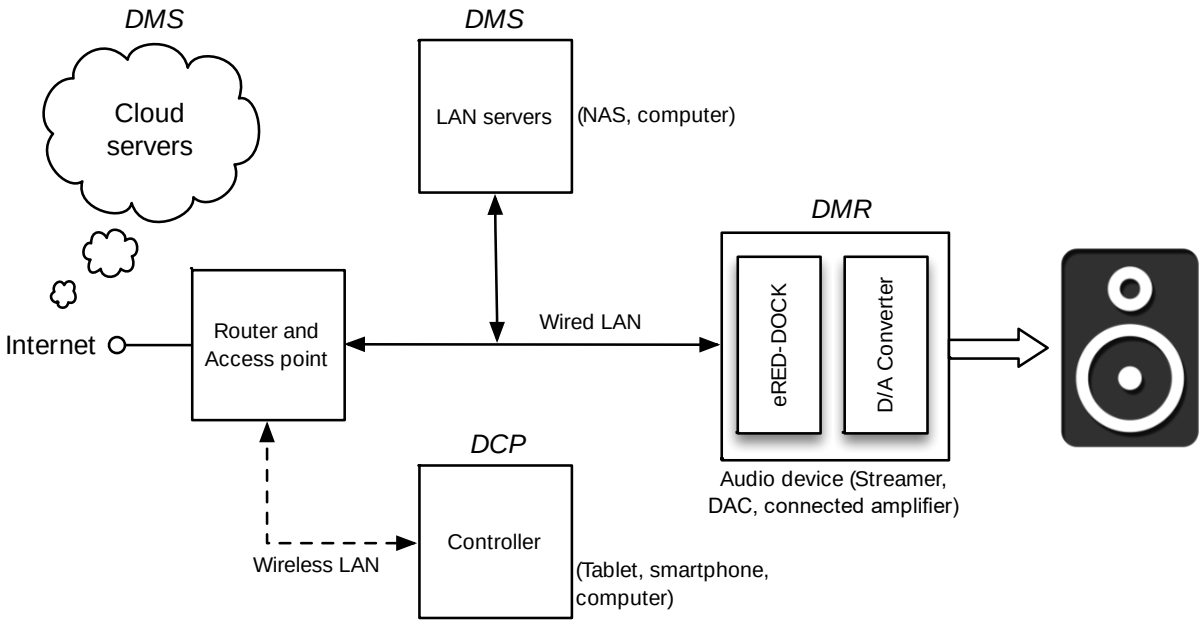

Figure 1-2 - Typical Network Audio Setup

1.5 Audio Formats

The design supports both multi-bit PCM (Pulse-Code Modulation) and one-bit DSD (Direct Stream Digital) modulations.

The following stereo audio formats are supported and decoded by the eRED-DOCK interface:

- WAV (Waveform Audio File Format)
- AIFF (Audio Interchange File Format)
- FLAC (Free Lossless Audio Codec)
- ALAC (Apple Lossless Audio Codec)
- APE (Monkey's Audio)
- WMA (Windows Media Audio)
- MP3 (Mpeg Audio Layer 3)
- AAC (Advanced Audio Coding)
- OGG Vorbis
- Uncompressed DSF and DFF (DSD stream file)

Standard WAV and AIFF files contain uncompressed pulse-code modulation (PCM) audio data. Like any non-compressed, lossless format, it uses much more disk space than compressed formats. Such uncompressed PCM streams are supported up to 384 kHz / 32-bit.

FLAC is an open format with royalty-free licensing. It supports for metadata tagging, album cover art, and fast seeking. The technical strengths of FLAC compared to other lossless formats lies in its ability to be streamed and decoded quickly, which is independent of compression level. Since FLAC is a lossless scheme, it is suitable as an archive format for owners of CDs and other media who wish to preserve their audio collections. The eRED-DOCK decodes FLAC files up to a sampling rate of 384kHz.

ALAC is an open source and royalty-free lossless audio codec developed by Apple Inc. It is frequently stored in MP4 file format container.

Monkey's Audio is a free, but not open-source lossless audio codec, relatively slower in encoding and decoding files compared to FLAC and ALAC.

WMA refers to a collection of audio codecs and formats developed and licensed by Microsoft.

MP3 and AAC are lossy compressions and encoding schemes for digital audio. These are non-free codecs covered by patents and subject to licensing by the final product manufacturer. The eRED-DOCK offers the technical ability to decode such formats, but engineered SA is not responsible for non-free audio codecs licensing.

Vorbis is free and open-source lossy compression audio codec with royalty-free licensing. It is commonly used with the Ogg file format container and referred to as Ogg Vorbis.

DSF and DFF files may contain multi-channel audio data and various resolutions. The eRED-DOCK supports uncompressed one-bit stereo audio at 2.8224 MHz, 5.6448 MHz and 11.2896 MHz

1.5.1 Licenses

It is the responsibility of the manufacturer of the final product (the brand) to take care of the licensing and fees for the non-free audio codecs.

The table and references below are provided for information purposes:

Format	License type	License	Owner	Info
WAVE	free	None (public domain)	Microsoft & IBM	Unlicensed [1]
AIFF	free	None (public domain)	Apple	Unlicensed [2]
FLAC	open	BSD / GPL2 / LGPL2	Xiph.Org Foundation	BSD
ALAC	open	Apache License 2.0	Apple	[3]
APE	free	None	Monkey's Audio	[4]
WMA	closed	Pay on volume	Microsoft	[5] and [6]
MP3	free	None	Fraunhofer IIS	[7]
AAC	closed	Pay on volume	MPEG Consortium	[8] and [9]
OGG	open	BSD-like	Xiph.Org Foundation	
DSF	open	None	Sony/Philips	Contact [10]
DFF	open	None	Sony/Philips	Contact [10]

Table 1-1 – Audio formats licenses

[1] Library of Congress, «WAVE Audio File Format,» 10 March 2020. [En ligne]. Available: https://www.loc.gov/preservation/digital/formats/fdd/fdd000001.shtml.

[2] Library of Congress, «AIFF (Audio Interchange File Format),» 27 July 2017. [En ligne]. Available: https://www.loc.gov/preservation/digital/formats/fdd/fdd000005.shtml.

[3] Apple Inc., «Apple Lossless Audio Codec,» 2011. [En ligne]. Available: https://alac.macosforge.org.

[4] Monkey's Audio, «License Agreement,» 2000. [En ligne]. Available: https://monkeysaudio.com/license.html.

[5] Microsoft, «Developing a Windows Media Audio or Windows Media Video implementation on a non-Windows platform,» 2020. [En ligne]. Available: https://www.microsoft.com/en-us/legal/intellectualproperty/tech-licensing/programs?activetab=pivot1:primaryr10.

[6] Microsoft, «Licensees Lists,» 2019. [En ligne]. Available: http://public.wmlalicensing.com/public/licensees-lists.aspx.

[7] Fraunhofer Institute for Integrated Circuits, «Alive and Kicking – mp3 Software, Patents and Licenses,» 18 May 2017. [En ligne]. Available: https://www.audioblog.iis.fraunhofer.com/mp3-software-patents-licenses.

[8] Via Licensing, «AAC Advanced Audio Coding,» 2019. [En ligne]. Available: https://www.via-corp.com/licensing/aac/.

[9] Via Licensing, «AAC License fees - standard rate and alternative rate structures,» 2019. [En ligne]. Available: https://www.via-corp.com/acc-license-fees-structures/.

[10] Sony, «Direct Stream Digital,» 2018. [En ligne]. Available: https://www.sony.net/Products/DSD/.

2 Characteristics and Specifications

2.1 Electrostatic Discharge Warning

Many of the components in this product are subject to be damaged by electrostatic discharge (ESD). Customers are advised to observe proper ESD precautions when unpacking and handling the board, including the use of a grounded wrist strap at an approved ESD workstation.

Caution: Failure to observe ESD handling procedures may result in damage to the product.

2.2 Recommended Operating Conditions

Table 2-1 indicates the recommended conditions under which the product should run properly.

Parameter	Recommend Condition
Power supply voltage	5.00 VDC
Operating free-air temperature	$T_{A(min/max)}$: 0 °C / 60 °C

Table 2-1 – Recommended operating conditions

2.3 Absolute Maximum Ratings

The user should be aware of the absolute maximum operating conditions for the eRED_DOCK interface. Failure to comply with these conditions may result in damage to the product. The minimum and maximum values are indicated in Table 2-2.

Parameter	Min.	Max.
Power supply voltage	-0.30 V	5.50 V
Input signal voltage	-0.30 V	5.50 V

Table 2-2 – Absolute maximum ratings

2.4 Electrical Specifications

Parameter	Min.	Typ.	Max.	Unit
External DC supply voltage	4.50	5.00	5.50	V
External DC supply current		350	500	mA
CMOS output high level V_{IH}	2.7	3.10	3.30	V
CMOS output low level V_{IL}	0	0.20	0.40	V
Differential S/PDIF output voltage [output loaded with 75Ω]		0.50		V
S/PDIF output impedance		75		Ω
Differential AES/EBU output voltage [Output loaded with 110Ω]		3.40		V
AES/EBU output impedance		110		Ω

Table 2-3 – Electrical specifications

2.5 Audio Resolution Specification

Parameter	Min.	Typ.	Max.	Unit
PCM digital audio resolution	16		32	bit
PCM digital audio sample rate	32		384	kHz
PCM digital audio dynamic range		32		bit
DSD sample rate	2.8224		11.2896	MHz

Table 2-4 – Audio resolution specifications

2.6 Master Clock Generator Specifications

Specifications here below show typical performances of the complete Master Clock generator circuit, including oscillators, multiplexer and fanout buffer.

Parameter	Min.	Typ.	Max.	Unit
Oscillator frequency stability, all inclusive (temperature, tolerance, aging, supply & load)			+/-50	ppm
Phase noise at 10Hz		-102		dBc/Hz
Phase noise at 100Hz		-132		dBc/Hz
Phase noise at 1kHz		-148		dBc/Hz
Phase noise at 10kHz		-155		dBc/Hz
Phase noise at 100kHz		-158		dBc/Hz

Table 2-5 – Master Clock generator specifications

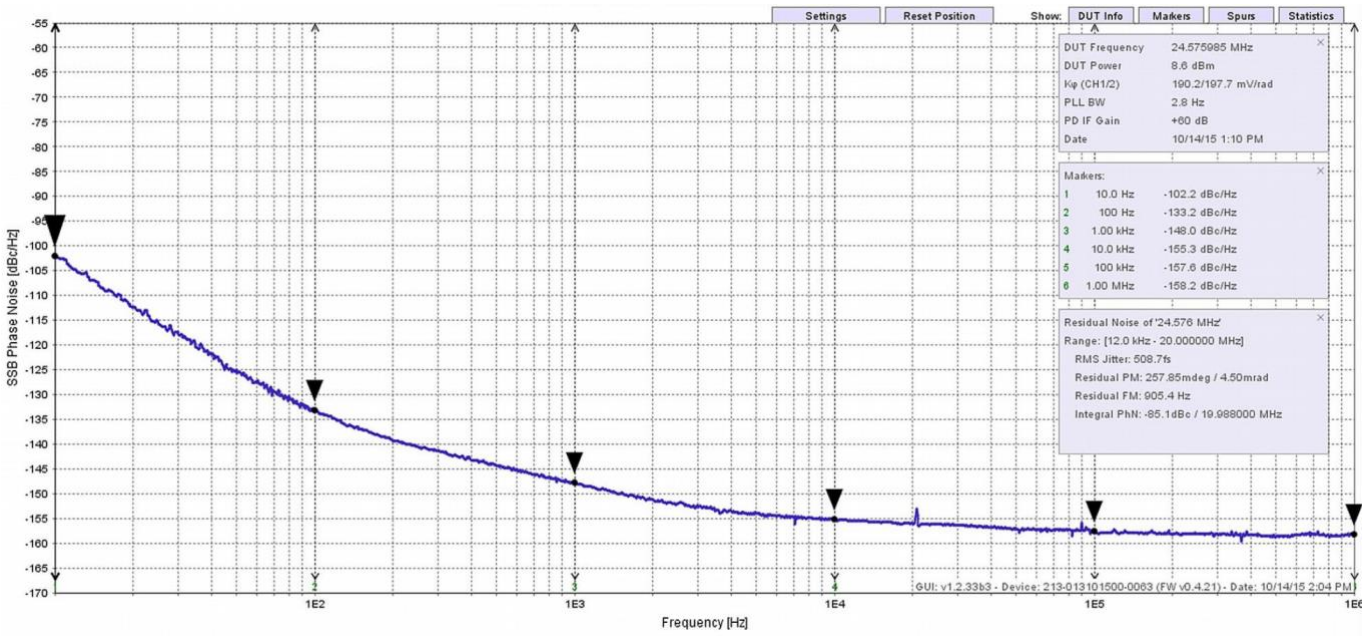

Figure 2-1 - Master Clock generator phase noise plot

3 Connectors Description

Please refer to Figure 5-1 for connectors location on the eRED-DOCK board.

3.1 I2S Connector [J7]

Industry standard connector for flat cable, 2.54mm pitch, 20-pos, 3M 2500-series.
Output level: CMOS compliant, refer to Electrical Specifications in chapter 2.4.

Pin #	Name	Type	Description
1	GND	Ground	Ground for I/O and clock management.
2	MCLK	Output	Master Clock Output – Master clock output at 22.5792MHz or 24.576MHz. Refer to Table 4-2.
3	GND	Ground	Ground for I/O and clock management.
4	SPDIF	Output	S/PDIF Output – Serial encoded PCM audio data stream, TTL level.
5	GND	Ground	Ground for I/O and clock management.
6	BCLK	Output	Serial Audio Bit Clock Output – Serial bit clock for PCM and DSD audio data.
7	GND	Ground	Ground for I/O and clock management.
8	PCM_LRCLK	Output	Serial Audio Left/Right Clock Output – Frame sync clock for PCM audio data.
9	GND	Ground	Ground for I/O and clock management.
10	PCM_SDATA1 /DSDR	Output	Serial Audio Data Output DSD right-channel audio data.
11	GND	Ground	Ground for I/O and clock management.
12	PCM_SDATA0 /DSDL	Output	Serial Audio Data Output Stereo PCM audio data / DSD left-channel audio data.
13	GND	Ground	Ground for I/O and clock management.
14	MUTE#	Output	Mute signal Low: the audio data stream is not valid and the DAC must be muted. High: the audio data stream is valid.
15	DSD_PCM#	Output	Audio Stream Format Low: the digital audio output stream format is PCM. High: the digital audio output stream format is DSD.
16	44K1_EN#	Output	Sampling Frequency Low: the sampling frequency is a multiple of 44.1kHz. High: the sampling frequency is a multiple of 48kHz. Refer to Table 4-1.
17	RATE0	Output	Sampling Rate – Sampling rate information. Refer to Table 4-1.
18	RATE1	Output	Sampling Rate – Sampling rate information. Refer to Table 4-1.
19	*reserved*	-	Unused. Do not connect.
20	GND	Ground	Ground for I/O and clock management.

Table 3-1 – I2S Connector description

3.2 Master Clock Output Connector [J2]

SMB coaxial male jack, Cinch Connectivity Solutions Johnson ref. 131-3701-261
Suggested matching female receptacle: Cinch Connectivity Solutions Johnson ref. 131-3403-101.
Suggested matching cable: Cinch Connectivity Solutions Johnson ref. 415-0004-006 or 415-0004-012.

Output level: 1.60V typical [50Ω load]
Output Impedance: 50Ω

Pin #	Name	Type	Description
1/Inner	Master Clock	Output	Master Clock Output at 22.5792MHz or 24.5760MHz
2/Outer	GND	Output	Ground

Table 3-2 – Master Clock Output connector description

3.3 S/PDIF Connector [J4]

Vertical Tail Pin Header, 2.54mm pitch, 2-Pos, type Harwin Inc. M20-series

Output level (S/PDIF compliant): 0.50Vpp [75Ω load]
Fully floating, transformer coupled
Output Impedance: 75Ω

Pin #	Name	Type	Description
1	SPDIF neg.	Output	S/PDIF Negative Output – Serial encoded audio data stream, buffered for coaxial cable connection.
2	SPDIF pos.	Output	S/PDIF Positive Output – Serial encoded audio data stream, buffered for coaxial cable connection.

Table 3-3 – S/PDIF connector description

3.4 AES/EBU Connector [J3]

Vertical Tail Pin Header, 2.54mm pitch, 3-Pos, type Harwin Inc. M20-series

Fully floating, transformer coupled
Output level (AES/EBU compliant): 3.40Vpp on 150Ω.

Pin #	Name	Type	Description
1	unused	-	Unused. Do not connect.
2	AES/EBU pos.	Output	AES/EBU Positive Output – Serial encoded audio data stream, buffered for balanced cable connection.
3	AES/EBU neg.	Output	AES/EBU Negative Output – Serial encoded audio data stream, buffered for balanced cable connection.

Table 3-4 – AES/EBU connector description

3.5 Power Supply Connectors [J5 and J6]

Male Header, horizontal, 2-pos, 3.0mm pitch, Molex Micro-Fit ref. 0436500200
Corresponding box for contacts: Molex 43645-0200

Alternative (parallel connection on Xu2S PCB):
Screw Terminal, 2-pos, 3.81mm pitch, Phoenix Contact 1985823
Corresponding Wire Gauge: 16-30 AWG

Pin #	Name	Type	Description
1	GND	Ground	Electrical ground.
2	VDD	Power	Power Supply Input +5.0 VDC.

Table 3-5 – External power supply connector description

Caution: Failure to respect the power supply polarity and voltage level may result in damage to the components.

3.6 Serial Peripheral Interface [J11]

Vertical Tail Pin Header, 2.54mm pitch, 2 x 3-Pos, type Harwin Inc. M20-series
Output level: CMOS compliant, refer to Electrical Specifications in chapter 2.4.

Pin #	Name	Type	Description
1	GND	Ground	Electrical ground.
2	SPI_SCK	Input	SPI Clock – Synchronous clock for serial data transmission and reception.
3	SPI_MOSI	Input	SPI Data Input – Serial data from the master MCU to the Renderer.
4	SPI_INT#	Output	SPI Interrupt Line – Active low, goes from high to low when the Renderer requests a communication.
5	SPI_CS#	Input	SPI Slave Select – Active low, used to communicate with the Renderer.
6	SPI_MISO	Output	SPI Data Output – Serial data from the Renderer to the master MCU.

Table 3-6 – AES/EBU connector description

4 Application Information

4.1 Galvanic isolation

The eRED-DOCK interface uses an RJ45 connector jack with integrated magnetics. The magnetics protect against faults and transients, including rejection of common mode signals between the transceiver and the cable. These signals are commonly caused by electromagnetic interference (EMI), either from noise picked up by the cable or from slight impedance mismatches. The magnetics also provide galvanic isolation from Ethernet cables, and offset any DC biasing caused by connected nodes having been powered from different sources.

Furthermore, both S/PDIF and AES/EBU outputs are fully isolated with wideband-RF transformers.

4.2 Master Clock Synchronisation

Asynchronous clocking allows for a full control of the network data transfer and audio master clock to minimize jitter and get the highest digital audio playback quality.

The onboard oscillators and clock management circuit have been designed together with a partner specialized in clocking devices. It is carefully optimized for audio and offers high performances, with an extremely low phase noise in the audio band. Please refer to chapter 2.6 and Figure 2-1 for detailed performance specifications.

For optimal results, we recommend using the eRED-DOCK Master Clock output to drive the Clock Input of the attached D/A converter circuit. Figure 4-1 illustrates a possible eRED-DOCK integration with a DAC board.

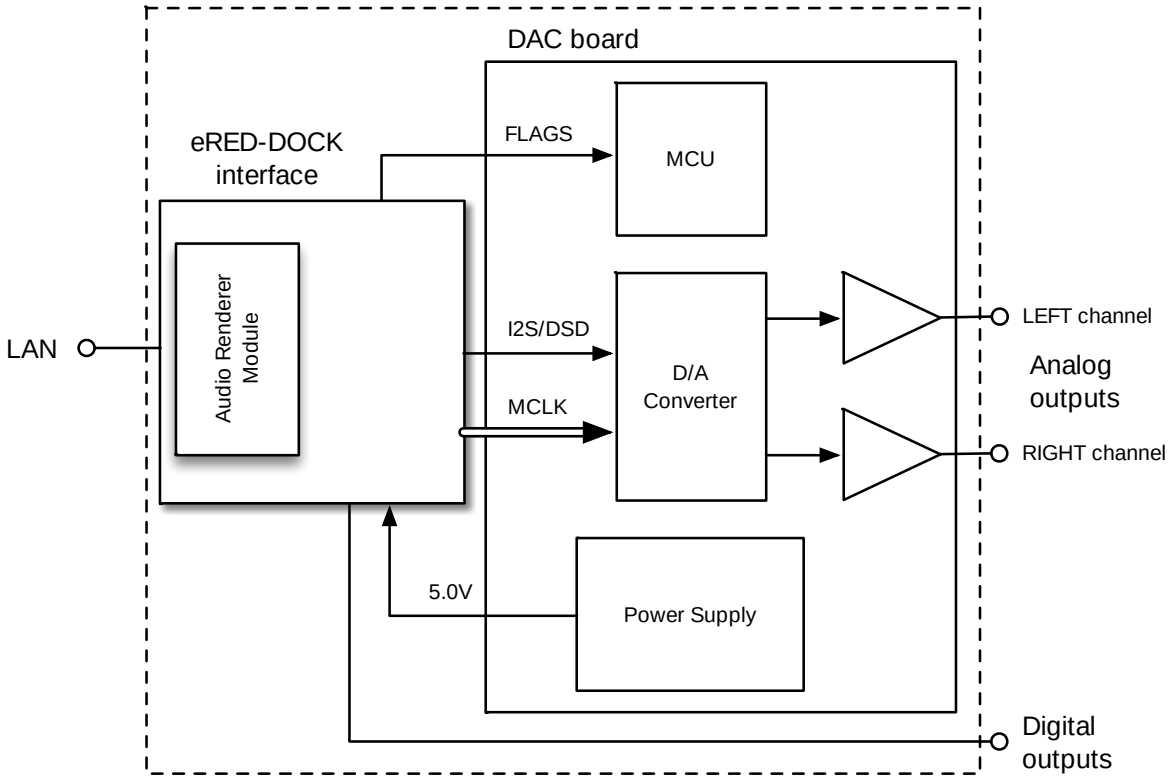

Figure 4-1 - eRED-DOCK integration with a DAC board

4.4 AES/EBU and S/PDIF Outputs

S/PDIF output is available on the 20-pole connector at standard CMOS level. Additionally, two buffered and isolated outputs for direct coaxial cable connection are provided. Fast drivers coupled to a very high-quality RF transformer ensures signal quality and integrity with standard 75Ω coaxial cables for S/PDIF and 110Ω balanced cabled for AES/EBU.

AES/EBU and S/PDIF standards support PCM up to 192kHz. Higher sampling rate such as 352.8kHz and 384kHz are not supported. For these formats, the I2S digital audio bus on the I2S Connector must be used.

Similarly, DSD cannot be transmitted over S/PDIF. The eRED-DOCK supports native DSD data for straight connection to a DSD-compatible DAC via the I2S Connector.

4.5 I2S Digital Audio Bus

Both S/PDIF and I2S ports are configured in master mode, thus the eRED-DOCK supplies audio data signal, Left/Right clock and Bit clock. Refer to section 4.6 for pin mapping and information relative to DSD mode.

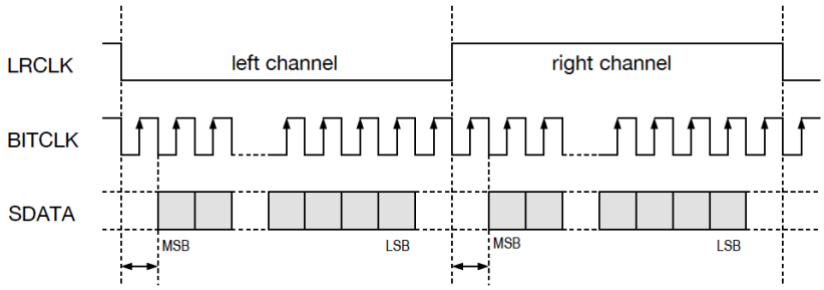

Figure 4-2 - I2S data format

The sampling frequency depends on the audio source track currently playing and media server configuration. It can be retrieved with the help of the hardware flags RATE0, RSTE1 and 44K1_EN# available on the I2S Connector pin 16 to 18. Monitoring of these flags is useful for updating the DAC configuration, or any post-processing settings whenever needed.

The MUTE# signal indicates that the serial data are no longer valid and therefore should be discarded. In order to avoid switching noise, the DAC shall be muted according to the MUTE# signal and during sampling rate or data format change.

Left/Right Clock Frequency (Fs)	RATE0	RATE1	44K1_EN#
44.1 kHz	High	High	Low
48 kHz	High	High	High
88.2 kHz	Low	High	Low
96 kHz	Low	High	High
176.4 kHz	High	Low	Low
192 kHz	High	Low	High
352.8 kHz	Low	Low	Low
384 kHz	Low	Low	High

Table 4-1 – Relation between sampling frequency and hardware flags

Table 4-2 shows how the audio sampling frequency (Fs), the bit clock frequency and the master clock frequency are related.

Left/Right Clock Frequency (Fs)	Bit Clock Ratio	Master Clock Ratio	Master Clock Frequency
44.1 kHz	64 · Fs	512 · Fs	22.5792 MHz
48 kHz	64 · Fs	512 · Fs	24.576 MHz
88.2 kHz	64 · Fs	256 · Fs	22.5792 MHz
96 kHz	64 · Fs	256 · Fs	24.576 MHz
176.4 kHz	64 · Fs	128 · Fs	22.5792 MHz
192 kHz	64 · Fs	128 · Fs	24.576 MHz
352.8 kHz	64 · Fs	64 · Fs	22.5792 MHz
384 kHz	64 · Fs	64 · Fs	24.576 MHz

Table 4-2 – Relation between left/right clock, master clock and bit clock

4.6 DSD mode

Support for native, uncompressed DSD64, DSD128 and DSD256 is provided by the eRED-DOCK interface. DSD data format is indicated by the flag DSD_PCM# on I2S Connector pin 15.

DSD_PCM#	Data Stream Type
Low	PCM
High	DSD

Table 4-3 – Data stream type

Table 4-4 shows how the DSD frequency is indicated by the hardware flags, and Table 4-5 illustrates the relation between DSD rate, Bit Clock and Master Clock frequencies.

DSD Type	RATE0	RATE1	44K1_EN#
DSD 64	High	High	Low
DSD 128	Low	High	Low
DSD 256	Low	Low	Low

Table 4-4 – Relation between DSD rate and hardware flags

DSD Type	Bit Clock Frequency	Master Clock Frequency
DSD 64	2.8224 MHz	22.5792 MHz
DSD 128	5.6448 MHz	22.5792 MHz
DSD 256	11.2896 MHz	22.5792 MHz

Table 4-5 – Relation between DSD rate, bit clock and master clock

In DSD mode, PCM_SDATA0/DSDL outputs left-channel DSD data and PCM_SDATA1/DSDR outputs right-channel DSD data. PCM_LRCLK must be discarded.

4.7 MUTE# signal

The MUTE# signal (active low) indicates that the serial data are no longer valid and therefore should be discarded. In order to avoid switching noise, the DAC shall be muted according to the MUTE# signal during sampling rate or data format change.

4.8 Serial Peripheral Interface

The eRED-DOCK interface features a full-duplex serial port based on the Serial Peripheral Interface standard.

The SPI port communicates in slave mode. It is used to access registers allowing the Audio Render Module to transmit information to the host device, referred as master, and to be configured for the desired operational mode. An interrupt line is provided to indicate a data change and avoid the need for the host to poll the interface continuously. The operation of the SPI port may be completely asynchronous with respect to the audio stream rates.

The SPI port is a five-wire serial interface where SPI_CS# (active low) is the module chip select signal, SPI_SCK is the control port serial clock from the master device, SPI_MOSI is the input data line from master, SPI_MISO is the output data line to the master and SPI_INT is the interrupt line.

Refer to the Audio Renderer Module datasheet for detailed description of the SPI and register interface.

4.9 Network Connexion

The eRED-DOCK is compatible with the UPnP AV/DLNA specification, and no specific user configuration is required to integrate it into an Ethernet network. There must be a DHCP server on the network where the eRED-DOCK operates so that it can fetch its IP address.

Basic boot status is provided by two signals, as indicated in the table below. These signals can be directly connected to status LEDs for diagnostic.

LED_S1	LED_S0	Description
1	1	Power up, booting
1	0	System booted, waiting for DHCP server
0	1	System booted and network configured, ready to operate
0	0	System Idle

Table 4-6 – status LED description

4.10 Configuration web page

Accessing the eRED-DOCK configuration web page requires a computer or any device with a web browser connected on the same network. The last digits of the renderer's IP address are indicated at the end of its UPnP *friendly name*. This allows to access the web page by introducing its IP address into a web browser, but most of the UPNP control apps offer a direct link to the page.

The eRED-DOCK configuration web page provides an interface for Firmware Update and customizing the renderer's UPnP *friendly name*.

5 Hardware Information

5.1 Connectors and Jumpers Location

The drawing here below shows where the LED's and connectors are located on the board.

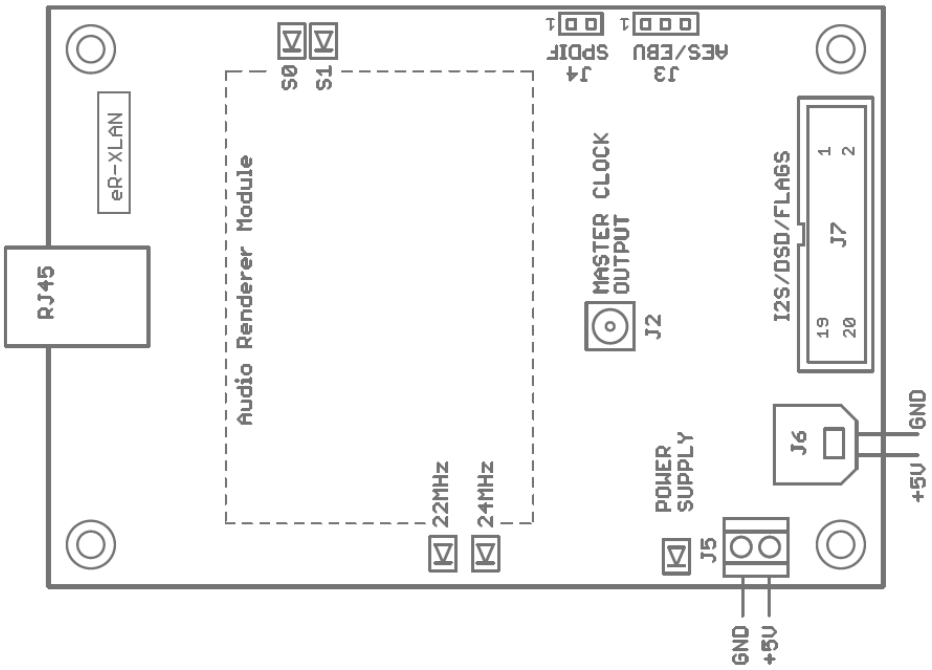

Figure 5-1 – Connectors and LED's location

5.2 Clock Termination Guidelines

This note is intended to provide basic guidelines necessary to allow end-users to properly interconnect the eRED-DOCK Master Clock 50Ω Output to CMOS-input D/A converter chip using SMB connectors. Figure 5-2 shows the basic termination circuit. Component's selection is discussed hereafter.

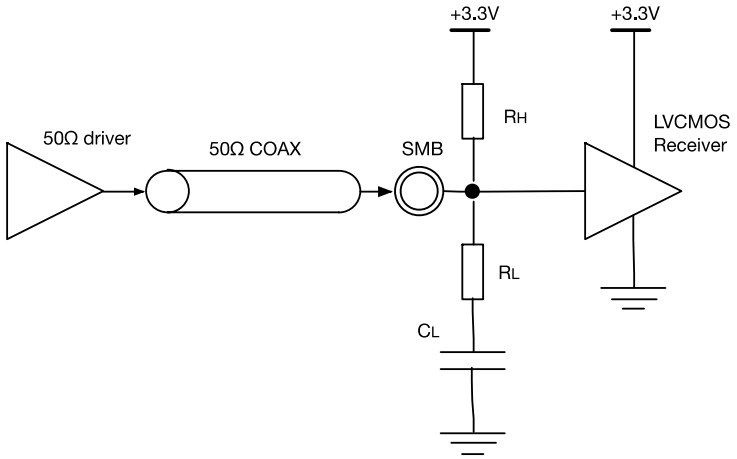

Figure 5-2 – Termination Concept

5.2.1 High Impedance

$R_H = R_L = \infty$

This Source Termination method is a very common way for single receiver, point-to-point situation. Although this works with standard LVCMOS inputs, it is not the best option regarding signal integrity and jitter.

5.2.2 50Ω Termination

The equivalent impedance is given by R_H and R_L in parallel, such as R_H and R_L form a 50Ω impedance. From signal integrity point of view, this is the traditional way to do it. We can consider 2 options:

a) $R_L = 50\Omega$, $R_H = \infty$
With C_L shorted, the clock signal amplitude at the receiver input stays between 0V and VDD/2. This situation is not compatible with usual LVCMOS inputs.

Adding C_L helps as the signal is now centered on VDD/2. However, if the driver goes into high impedance, the receiver input is floating.

b) $R_L = 100\Omega$, $R_H = 100\Omega$
With C_L shorted, the clock signal amplitude at the receiver input is between 0.25VDD and 0.75VDD. This situation is optimal if the receiver switching levels are 30% and 70%.

The receiver input is at VCC/2 if the driver goes into high impedance (CMOS input gates draw more current in this case). Adding C_L solves this issue by pulling the line to VDD in driver OFF state, but the active signal is then shifted between 0.40VDD and 0.90VDD which may be again not compatible with LVCMOS inputs.

In the above circuit options, capacitor C_L shall be calculated so that its impedance at the operating frequency is less than 5Ω.

5.3 Board Dimensions

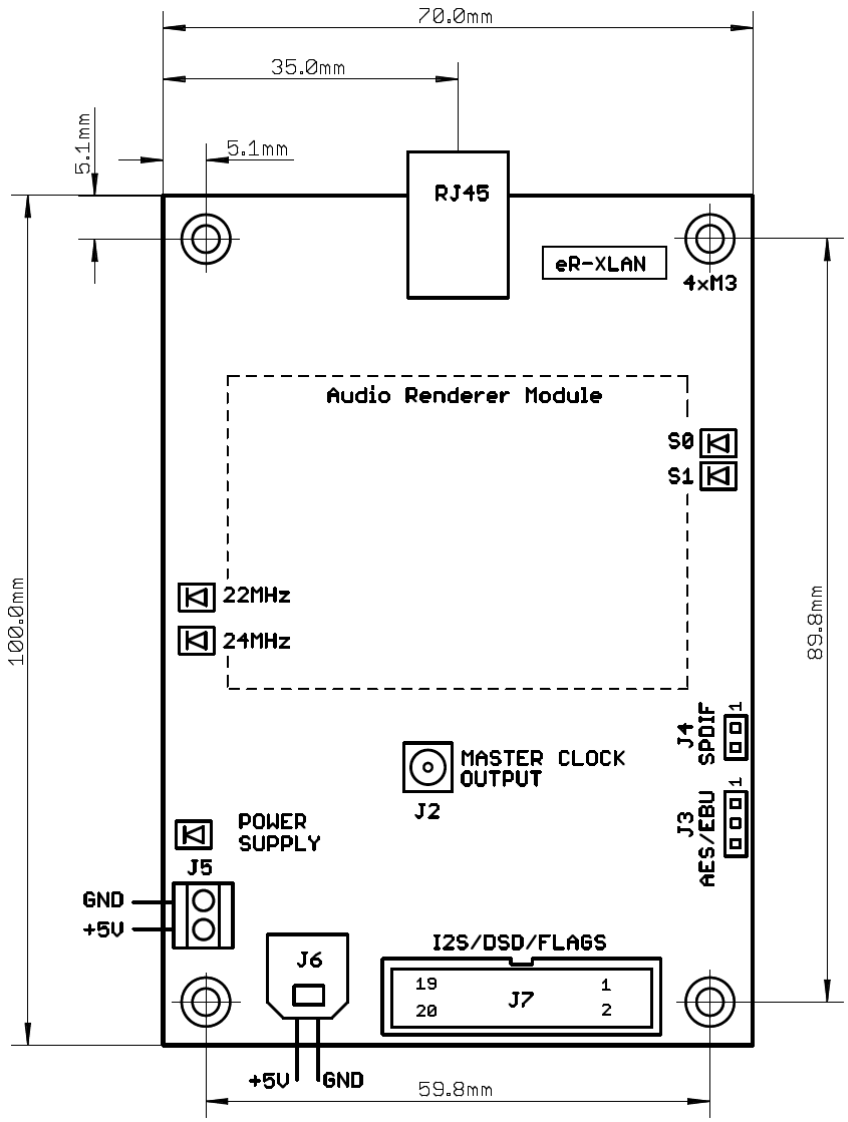

Figure 5-3 – Mechanical dimensions in millimeters

6 Ordering Information

6.1 Part Number

Part Number	Description
eRED-DOCK	Network Digital Audio Playback Interface